**FEATURES**

- Home Networking Analog Front End IC covering HomePNA 3.1 and Broadband PLC (HD-PLC, HPAV, etc)
- High speed sampling rate and low power consumption
- High resolution and wide frequency range
- Up to 80MSPS data rate
- Tx path
  - 12bit 160MSPS DAC with 0.5dB gain step
  - x2 interpolation filter
  - Configurable SSB modulation
  - Integrated maximum 20.3dBm current sink line driver with 1dB gain step
- Rx path
  - 12bit 160MSPS ADC
  - /2 decimation filter
  - Configurable SSB modulation
  - -18 dB to +42dB low-noise PGA with 1dB gain step
  - 14MHz - 90MHz configurable LPF cutoff frequency
- Internal clock multiplier (PLL)
- Integrated fine and accurate foreground calibration on Tx and Rx path
- 64 Exposed Quad Flat No-Lead package (VQFN)

**GENERAL DESCRIPTION**

The KHN11112 is a highly integrated analog front-end IC (AFE) for the home networking applications such as HomePNA and broadband/narrowband PLC. Data rates up to 80MSPS are supported in both Rx and Tx paths. SPI (serial peripheral I/F) allows software programmability of the AFE.

The functional block diagram of the KHN11112 is shown in Fig1. The Tx signal path consists of a x2 low-pass interpolation filter, 12-bit 160MSPS DAC, and line driver (IAMP). The interpolation filter has a high-pass and low-pass mode and can be bypassed. In high-pass mode, typical signal band is between 36MHz and 52MHz, and is between 2MHz and 36MHz in low-pass mode. The DAC is foreground calibrated to ensure 12-bit static accuracy. The line driver delivers 20.3 dBm signal power (84.8mA). Tx power can be controlled over a 20dB range with 0.5dB step.

The Rx signal path consists of a programmable amplifier (PGA), a 160MSPS ADC and a decimation filter to generate a 80MSPS digital output word. The low-noise PGA has a programmable gain range of -18dB to +42dB in 1dB steps. Its input referred noise is less than 3 nV/√Hz for gain settings beyond 30dB. The LPF cutoff frequency is configurable between 14MHz and 90MHz. DC tune circuits are implemented to reduce the offset with the accuracy of ±5%. De-emphasis is foreseen to compensate for high-frequency losses in the line and PGA stages. An option to bypass the decimation filter is also available for AGC and test purposes.

On-chip PLL multiplier and synthesizer provide all the required clock signals from a single crystal or clock source. The 12-bit digital data interface runs maximum of 80MHz in half-duplex mode, and up to 108MHz in full duplex mode. The KHN11112 is available in a 64 Quad Flat No-Lead package (VQFN), 9mmx9mm with 0.5mm pin pitch. It is specified over the industrial temperature range of -40°C to +85°C.

**BLOCK DIAGRAM**

![Functional block diagram](KHN11112.png)

**Fig1. Functional block diagram**

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